



G.P. 12816
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T.J. Gabara 80

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Thaddeus J. Gabara
Case: 80
Serial No.: 09/870,436
Filing Date: May 30, 2001
Group: 2816
Examiner: Hai L. Nguyen

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature: Laura A. Haskin Date: September 25, 2002

Title: Comparator Circuits Having Non-Complementary Input Structures

AMENDMENT TRANSMITTAL

Assistant Commissioner for Patents
Washington, D.C. 20231

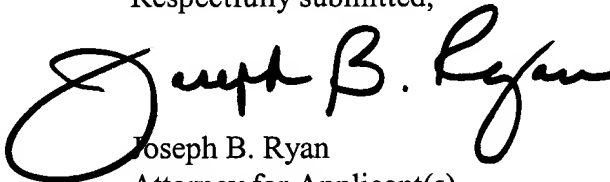
Sir:

Submitted herewith is the following document relating to the above-identified patent application:

(1) Amendment and Response to Office Action.

Please extend the period for response by two months to September 25, 2002. Please charge **Ryan, Mason & Lewis, LLP Deposit Account No. 50-0762** the amount of \$400, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter is enclosed.

Respectfully submitted,



Date: September 25, 2002

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Signature: Jesus L. Nolasco Date: September 25, 2002

Title: Comparator Circuits Having Non-Complementary Input Structures

AMENDMENT AND RESPONSE TO OFFICE ACTION

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

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In response to the outstanding Office Action dated April 25, 2002, please amend the above-identified application as follows:

IN THE CLAIMS

40. (Amended) A circuit comprising at least first and second input legs, the first and second input legs having non-complementary structures relative to one another, each of the non-complementary structures having associated therewith a variable parameter having a value that is a function of a corresponding input signal, a difference in the variable parameters associated with the first and second input legs being detectable in the circuit;

wherein at least one of the first and second input legs comprises a weighted array of transistors, each of the transistors in the weighted array adapted to receive a particular portion of an input signal applied to that leg.